ANALYSIS OF A NOVEL DEAD-TIME COMPENSATION TECHNIQUE FOR THREE PHASE SPACE-VECTOR PWM BASED VSI DRIVES

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ABSTRACT

Due to the finite turn on and turn off times of switching devices typically a dead-time is inserted in between the off going and turning on devices to prevent a shoot through in the DC link. Even though this assures safe operation several undesired attributes such as fundamental voltage drops, output waveform distortions & torque pulsations are also introduced as a result of this time delay. This paper introduces a novel dead time compensation technique for space vector PWM based voltage source inverters and also a detailed examination of the distortion caused by dead-time is presented. Using the proposed method dead-time is compensated accurately resulting a better frequency spectrum. Time domain and frequency domain results both are presented to verify the findings.

***Key words*:** Voltage Source Inverters, Space Vector PWM, Dead-Time

1. INTRODUCTION

With the recent development of the power electronic components, the PWM inverters gained its popularity in the industry. Due to its high efficiency and controllability of the output the PWM inverters were preferred in the industrial and commercial environment. Despite of these advantages, they still have to be improved for greater performance. Dead time distortion, Power device voltage drop and stator voltage drop are some of the major obstacles faced by the PWM inverters. Considerable effort is given in order to remove these drawbacks and improve the performance of the inverters.

When the PWM inverters are considered, the switching devices of the inverter have finite switching times. As a result there is a possibility of a shoot through in the DC link of the inverter which could induce serious damages to the inverter. A small time delay is inserted in between the switching pulses in order to prevent such accidents from happening. This delay is called the “Dead-time” delay [1]-[4]. Although the dead –time delay guarantees a safe operation, it causes some major issues in the output waveform of the inverter. This effect is called the “Dead time distortion”.

Over the years, considerable amount of time and resources have been invested upon solving the dead time distortion problem. Several different dead time compensation methods have been devised so far and some managed to correct the dead time distortion for a reasonable accuracy. In [2]-[4], the compensation is done by trying to make the magnitude of the output to be equal to the desired ideal output.

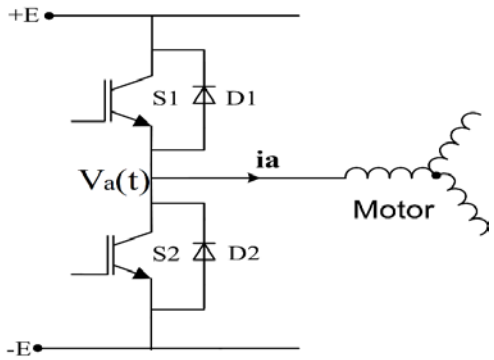

Figure 1: One Leg of the Three Phase PWM Inverter

But the output consists of an inherent phase lag which can be undesired in some industrial applications. This phase lag obstacle has been overcome by the method suggested in [5]. But this requires double sampling per carrier period which will eventually increase the processor overhead. Methods proposed in [6] & [7] handle the compensation accurately without any magnitude or phase distortions. But all the above mentioned techniques are based on sinusoidal PWM algorithm. By using Space vector PWM (SVPWM), the performance of the inverter can be further improved by improving the harmonic spectrum, increasing the linear modulation range

and reducing switching losses [8]. In this paper a novel dead time compensation technique based on the SVPWM is introduced and the validity of the method is illustrated using simulation results.

1.1 Dead-Time Effect

One leg of a three phase inverter is shown in Figure 1. S1 and S2 are the two IGBT switches which are in series with each other connecting the DC bus. The PWM pulses which are delayed by an amount of dead-time delay (Td) are fed into the S1 and S2. The switching pulses are shown in the Figure 2. The direction of the current shown in Figure 2 is considered as positive current direction. Figure 2(a) & 2(b) shows the ideal switching pulses which are fed into the IGBT switches S1 and S2 respectively. The pulses delayed by Td are shown in Figure 2(c) & 2(d). The rising edge of each pulse is delayed by an amount of Td. Since both S1 and S2 are in off state during dead time period, the output cannot be manipulated [7], [9]. Output depends on the current direction during this dead band. If the load current is positive, current will flow through diode D2 and the output will be equal to –E. Likewise for negative current the output will be equal to +E.

The resulting output pulses are illustrated in Figure 2(e) & 2(f). It can be clearly noticed that when the current is positive, there is a loss in the output pulses and when the current is negative, there is a gain compared to the ideal case[3],[5]. This gain and loss gives rise to an undesired deviation in the output waveform. This is called the dead-time effect [1]-[7]. As a result of this dead time effect, drawbacks like drops in the magnitude of the fundamental voltage and current components, output waveform distortions, increase of the harmonic distortion occurs [4], [5] & [7].

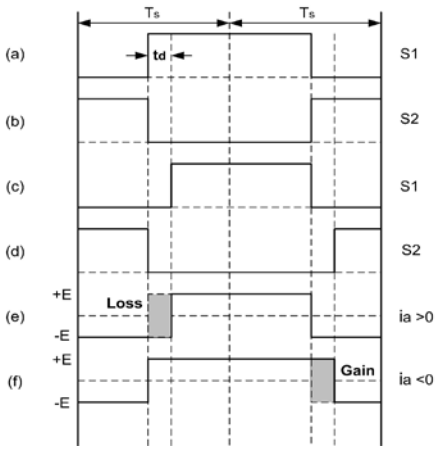

Figure 2: Distorted PWM gate signals

2. DEAD-TIME COMPENSATION

Proposed dead-time compensation technique is based on edge delaying concept since edge delaying is far less software and hardware intensive than edge advancing. Hence memory consumption and resource allocation is revamped in edge delaying compensation method.

2.1 Edge Delaying Compensation

Edge delaying compensation is widely used in PWM inverters due to its implementation ease. Despite its implementation easiness due to delaying each switching pulse at each cycle the output gets delayed by a certain amount. When output is delayed, in order to use feedback to improve the performance of motor drives, additional software & hardware components are required. To eliminate this delay a simple modification in PWM generation was derived in [7] for Sine PWM (SPWM) inverter motor drives. But for the betterment of the induction motor drive this work can be extended for space-vector PWM (SVPWM) as well.

In edge delaying the edges of the switching pulses are delayed depending on the direction of the phase current. When the current is positive (into the motor) the falling edge is delayed and when the current is negative (into the inverter) the rising edge of the switching pulse is delayed. The delay eliminating hysteresis loop requires a reference waveform and it's been derived for carrier based PWM. Therefore the relationship between carrier based PWM and SVPWM is used and symmetrical switching pulses are generated using the graphical representation of SVPWM.

2.2 PWM Generation

PWM signal generation can be classified in to two different categories as carrier based PWM and carrier less PWM. Generally the modulation signal in carrier based PWM is sinusoidal. But injection of zero-sequence signals for a three phase inverter has led to non-sinusoidal carrier based PWM. Distinct zero-sequence signals lead to distinct non-sinusoidal PWM modulators. Each of these PWM generation strategies significantly differ from each other. These PWM strategies have developed to have a wide linear modulation range, better harmonic spectrum and less total harmonic distortion (THD) in switching waveform and less switching losses.

SVPWM has become very popular for three phase inverters in parallel to the development of

microprocessors. It uses space-vector concept to calculate duty cycles for switches. SVPWM is known for its easy digital implementation, better harmonic spectrum, less THD and wide linear modulation range for output line-to-line voltages. Even though SVPWM is categorized as a carrier less PWM scheme, if the three phase inverter is used with a Y connected symmetrical load a relationship between space-vectors and zero sequence voltage (common mode voltage) can be drawn. Since this paper discusses about an induction motor drive the relationship is pragmatic because the load is an induction motor.

2.3 Symmetrical PWM Generation

Non-sinusoidal modulating signals can be generated by modifying the fundamental signal (Uaref, Ubref, Ucref) using a zero-sequence voltage (Zsv(t)). By choosing an apt Zsv(t) we can generate symmetrical PWM (SYPWM) signals. To generate SYPWM signals we select Zcv(t) to be the following. Umax is the possible maximum out of Uaref, Ubref & Ucref and Umin is the possible minimum out of Uaref, Ubref & Ucref at an instant.
Thus Zsv(t) can be generate as (01).

$$Z_{sv}(t) = 0.5 * (1 - U_{max}) + 0.5 * (-1 - U_{min}) \quad (01)$$

As shown in Figure 3. , using the fundamental signal and zero-sequence voltage the modulation signal (Uamod) can be generated. Generated signals are shown in Figure 4.Uamod can be used to generate the symmetrical pulses. But due to the inherent phase delay introduced by the edge delaying circuit the output will be delayed by Td amount.
Let

$$d = Uamod(t) - Ucarrier(t) \quad (02)$$

Using a hysteresis loop, provided d as its input the reference voltage can be altered.

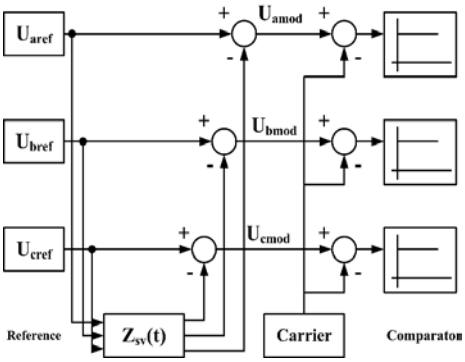

Figure 3: Symmetric PWM generation signals

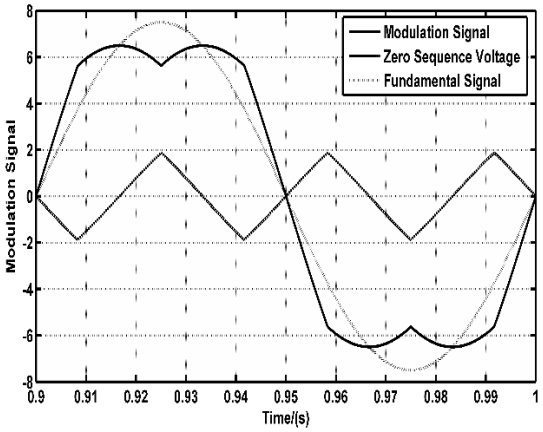

Figure 4: Symmetric PWM generation signals

2.4 Output Delay-Time Elimination

It is evident that if the original symmetric switching pulses were used to trigger the IGBTs the output will be delayed by a Td amount. Therefore to overcome this scenario a simple reference wave modification is made[7]. Due to the modification, the switching pulses gets advanced by a Td amount. If these already advanced pulses are used to switch the IGBTs, theoretically the output must be advanced by a Td amout. But due to the inherent time delay introduced by the edge delaying, the advancement and the delay will cancel each other out and ultimately the output will be coincided with the ideal output voltage. As disussed in [7] switching pulses can be modified using a simple pulse waveform (F(d)) shown in Figure 5(a) which is generated by a hyeteresis loop. When F(d) is substracted from Uamod the altered reference waveform can be obtained. Figure 5(b) shows the original switching pulse generated by using Uamod. Figure 5(c) shows advanced switching pulse generated by using Uamodref. When the already advanced pulse is used to fire the IGBTs the output delay time can be eliminated.

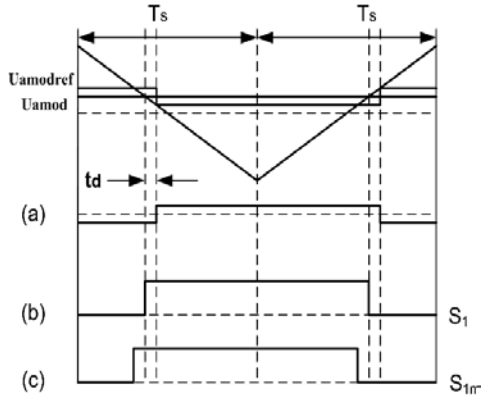

Figure 5: Phase Lag Elimination Method

3. RESULTS

In order to verify the validity of the proposed method simulations were carried out in MATLAB Simulink environment. Proposed method was used to drive a three phase induction motor. Parameters of the induction motor used is given in the Table 1. Simulations included a DC link, three phase PWM inverter and an asynchronous motor model.

For simulation 3hp induction motor was used. The added dead time delay was 40 us. Induction motor operating frequency was set to 10 Hz and carrier frequency to 1830Hz. DC link voltage was set to 135V. Amplitude of carrier wave was taken as 15V and modulation index ma was set to 0.5. If the voltage drop in fundamental voltage due to dead-time is ΔV. Easy calculation leads to $\Delta V = 2VcfcTd = 2.196$.

To analyze the impact and effectiveness of the proposed dead-time compensation method, amelioration of distorted phase currents is observed. The distorted current waveform of phase A due to dead-time is shown in Figure 6. Compensated steady state current waveform of phase A using the proposed method is shown in Figure 7. In order to investigate the harmonic spectrum the single sided frequency spectrum of phase A current is also taken in to consideration Figure 8. & 9.

Table 1: Induction Motor Parameters

Stator Resistance Rs	3.41	Stator Inductance Ls	0.1868
Rotor Resistance Rr	3.41	Mutual Inductance Lm	0.1728
Rotor Inductance Lr	0.1868	Number of pole pairs	2

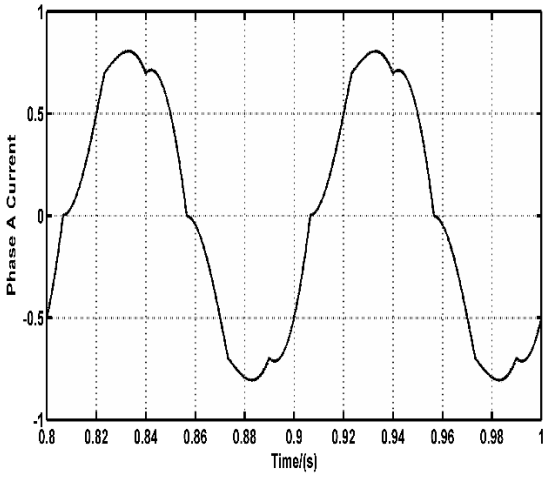

Figure 6: Distorted Phase A Current Waveform

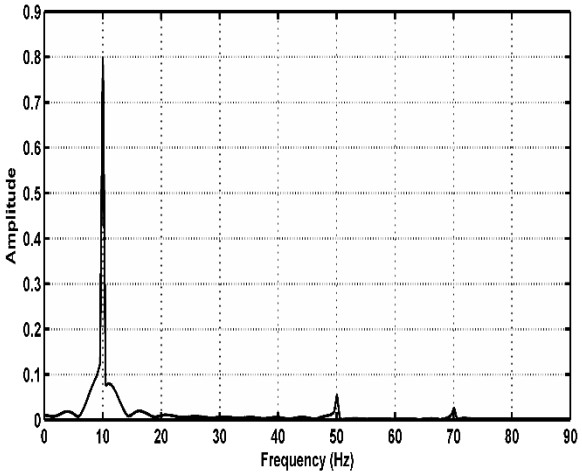

Figure 8: Single-Sided Amplitude Spectrum of Distorted Phase A Current

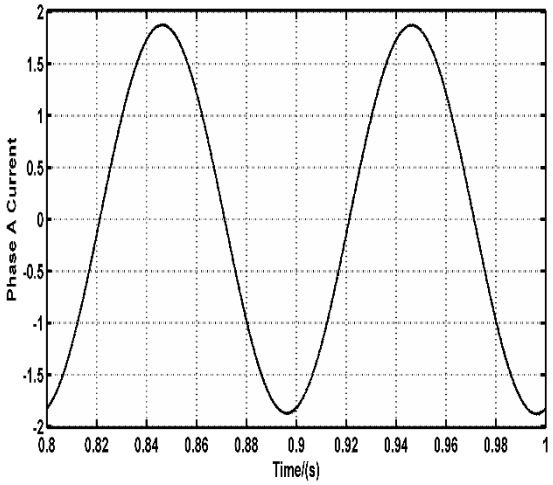

Figure 7: Compensated Phase A Current Waveform

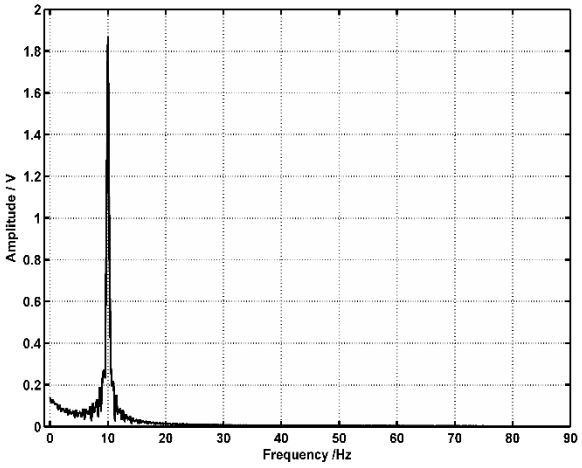

Figure 9: Single-Sided Amplitude Spectrum of Compensated Phase A Current

4. CONCLUSION

The dead time compensation method proposed in the paper provides a simple solution for the dead time distortion problem for SVPWM based three phase inverters. The correction is done by analyzing pulse by pulse in order to correct each pulse individually. The dead time compensation is done by a simple edge delay circuit and the phase lag introduced by the compensation method is removed by a simple modification to the reference wave. SVPWM switching pulses are obtained by zero sequence voltage injection. The compensation method accurately compensates the dead time distortion and the output waveforms are free of any phase delay errors. The validity of the method is confirmed by the simulation results. Current waveforms of compensated output and uncompensated output are provided in order to illustrate the improvement by the compensation method. Frequency spectrums of the distorted and compensated phase current waveforms are provided in order to investigate the harmonic mitigation.

In motor speed control applications harmonics should be avoided at all costs. Harmonics not only waste energy it is the root cause for torque pulsations. As it can be seen in Figure 8. the distorted current waveform contains several harmonics at different frequencies. When the motor operating especially at low frequencies these unwanted harmonics come in to play and torque pulsations are clearly visible due to the inertia effect. Figure 9. shows how the proposed method has improved the frequency spectrum of the phase current by eliminating 5^{th} and 7^{th} harmonics. Furthermore the amplitude of the fundamental is also gets reduced due to dead-time distortion. Fundamental current shown in Figure 8. has an amplitude of 0.8V but after compensating the dead-time the fundamental current shown in Figure 9. shows a clear increment of 1V.

In conclusion, the proposed dead-time compensation method compensates magnitude as well as the phase accurately. Moreover the SVPWM provides less harmonic distortion, less switching losses as well as a wide linear range.

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